CLAIMS

What is claimed is:

1. A method for manufacturing a multi-thickness gate dielectric layer of a semiconductor device, the method comprising:

forming a first dielectric layer on a semiconductor substrate;

forming a second dielectric layer on the first dielectric layer, the second dielectric layer having a different dielectric material from that of the first dielectric layer; and

selectively removing a portion of the second dielectric layer so as to selectively expose a portion of the first dielectric layer under the second dielectric layer to form a gate dielectric layer including a thick portion formed of the first dielectric layer and remaining second dielectric layer and a thin portion formed of the exposed first dielectric layer.

2. The method as claimed in claim 1, wherein the first dielectric layer or the second dielectric layer is formed of a material selected from the group consisting of: silicon oxide, silicon nitride, hafnium oxide, aluminum oxide, zirconium oxide, and tantalum oxide.

3. The method as claimed in claim 1, wherein the first dielectric layer is formed of thermal oxide.

4. The method as claimed in claim 1, wherein the first dielectric layer is formed of silicon oxide using rapid thermal oxidation.

5. The method as claimed in claim 1, wherein the first dielectric layer or the second dielectric layer is formed of hafnium oxide or aluminum oxide using atomic layer deposition.

6. The method as claimed in claim 1, wherein the selective removal of the second dielectric layer comprises:

applying a photoresist pattern on the second dielectric layer; and

etching the exposed second dielectric layer adopting a dry or wet etch process by using the photoresist pattern as an etch mask.

7. The method as claimed in claim 6, wherein the etching process is performed such that an etch rate of the second dielectric layer is higher than that of the first dielectric layer.

8. The method as claimed in claim 1, further comprising nitridizing a surface of the gate dielectric layer.

9. The method as claimed in claim 1, further comprising forming a third dielectric layer using a different dielectric material from that of the second dielectric layer, on the second dielectric layer; and

selectively removing a portion of the third dielectric layer so as to selectively expose the second dielectric layer under the third dielectric layer,

wherein the gate dielectric layer includes the remaining third dielectric layer, second dielectric layer, and first dielectric layer, which are stacked.

10. A method for manufacturing a multi-thickness gate dielectric layer of a semiconductor device, the method comprising:

forming a first dielectric layer on a semiconductor substrate;

forming a second dielectric layer on the first dielectric layer, the second dielectric layer having a different dielectric material from that of the first dielectric layer;

selectively removing a portion of the second dielectric layer so as to selectively expose a portion of the first dielectric layer under the second dielectric layer;

selectively removing a portion of the exposed first dielectric layer so as to selectively expose a portion of the semiconductor substrate under the exposed first dielectric layer; and

forming a third dielectric layer having a thickness that is thinner than that of the first dielectric layer on the exposed semiconductor substrate, to form a gate dielectric

layer including a thick portion formed of the first dielectric layer and remaining second dielectric layer, a medium-thickness portion formed of the exposed first dielectric layer, and a thin portion formed of the third dielectric layer.

11. The method as claimed in claim 10, wherein the first dielectric layer, the second dielectric layer, or the third dielectric layer is formed of a material selected from the group consisting of: silicon oxide, silicon nitride, hafnium oxide, aluminum oxide, zirconium oxide, and tantalum oxide.

12. The method as claimed in claim 10, wherein the first dielectric layer or the third dielectric layer is formed of thermal oxide.

13. The method as claimed in claim 10, wherein the first dielectric layer or the third dielectric layer is formed of silicon oxide using rapid thermal oxidation.

14. The method as claimed in claim 10, wherein the first dielectric layer, the second dielectric layer, or the third dielectric layer is formed of hafnium oxide or aluminum oxide using atomic layer deposition.

15. The method as claimed in claim 10, wherein the selective removal of the second dielectric layer comprises:

applying a first photoresist pattern on a portion of the second dielectric layer; and

primarily etching an exposed portion of the second dielectric layer adopting a dry or wet etch process by using the first photoresist pattern as an etch mask,

and wherein the selective removal of the portion of the exposed first dielectric layer comprises:

applying a second photoresist pattern covering the remaining second dielectric layer and the portion of the exposed first dielectric layer; and

secondarily etching a portion of the portion of the exposed first dielectric layer adopting a dry or wet etch process by using the second photoresist pattern as an etch mask.

16. The method as claimed in claim 15, wherein the primary etching process is performed such that an etch rate of the second dielectric layer is higher than that of the first dielectric layer.

17. The method as claimed in claim 10, further comprising nitridizing a surface of the gate dielectric layer.

18. The method as claimed in claim 10, wherein the third dielectric layer is formed by deposition to extend over the remaining second dielectric layer and first dielectric layer.

19. The method as claimed in claim 10, further comprising forming a third dielectric layer using a different material from that of the second dielectric layer, on the second dielectric layer; and

selectively removing a portion of the third dielectric layer so as to selectively expose a portion of the second dielectric layer under the third dielectric layer,

wherein the gate dielectric layer has the remaining third dielectric layer, second dielectric layer, and first dielectric layer, which are stacked.